Parkes–CDSCC Telemetry Array: Equipment Design

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A unique combination of DSN and non-DSN facilities in Australia provided enhanced data return from the Voyager spacecraft as it encountered the planet Uranus. Many of the key elements are duplicated from Voyager's encounters with Jupiter and Saturn. Some are unique extensions of that technology.

I. Introduction

The Parkes–CDSCC Telemetry Array (PCTA) utilizes the 64-m Australian Parkes Radio Telescope (Fig. 1) to augment the Canberra Deep Space Communication Complex (CDSCC) by some 50% to support the Voyager/Uranus encounter, and, if all goes well, for Neptune. This is based upon a CDSCC complement of one 64-m and two 34-m antennas, as well as a recent reflector surface upgrade at Parkes. This upgrade is part of the X-band preparation recently completed by the Commonwealth Scientific and Industrial Research Organization (CSIRO) and the European Space Agency (ESA) for the support of the Giotto mission. Arrangements have been made to share the common front-end electronics, such that the DSN implementation at Parkes does not impact the focal point equipment area. A dedicated two-way intersite link between Parkes and the CDSCC has been completed by Telecom Australia, under contract with the Australian Department of Science.

Together, these facilities provide the critical elements of a real-time combining system as utilized for past encounters with Goldstone's DSS-12 and DSS-14. To achieve this capability, a short-loop receiver, operating from a fixed frequency downconverter, is required at Parkes to extract the Voyager baseband signal. In addition, a third-generation baseband combiner is required at the CDSCC to accommodate the longer baseline. To complete the real-time system, a dedicated monitor and control capability offers improvements in operational reliability and convenience as compared to the combining systems in use for recent planetary encounters.

Because the Voyager Project has based its data return strategy upon the Parkes contribution, the real-time system is backed-up with baseband recordings at both sites, such that the tapes can be brought together for playback through the combiner (when and as required) within six hours of the end of pass. This near-real-time capability has been developed as a temporary modification to the Mark III Very Long Baseline Interferometry Data Acquisition Terminals scheduled in the near future for all DSN complexes. This recording capability creates redundancy for the intersite link and portions of the CDSCC electronics equipment.

II. System Description

Figure 2 is a functional block diagram of the system with its interfaces with ESA, CSIRO, Telecom, and the Mark IVA DSN at CDSCC. Mark IVA is the designated configuration of the DSN complexes in the latter half of this decade.

At the Parkes antenna, now in service for over 20 years, CSIRO has just completed a major upgrade in facilities, servo, pointing, and data processing computers and master equatorial. In addition, the reflector surface improvements on the antenna were designed for X-band performance approaching that of DSS-43 at high elevation angles, as is required for Voyager support.

A corrugated wide-illumination-angle focal point feedhorn (Fig. 3) has been designed and fabricated at CSIRO's Division of Radiophysics at Epping, New South Wales. This couples to the JPL-supplied microwave assembly (Fig. 4), a direct copy of the DSN 64-m design. This unit provides simultaneous right-hand circular polarization (RCP) and left-hand circular polarization (LCP) outputs to the following dual traveling wave masers (TWM) in such a manner that by rotating the polarizer, redundant TWM capability is available to the Giotto and Voyager RCP signals, as well as to the Voyager back-up LCP mode. The ESA-provided, U.S.-manufactured TWMs are of JPL Block II design. The international flavor of the front-end equipment is rounded out with the dual downconverter of French origin, all integrated at ESA's European Space Operations Center (ESOC) at Darmstadt, West Germany. The remaining non-JPL-provided equipment is the Telecom supplied video grade link of Japanese manufacture. In addition, a controller interface data link at 4800 baud is provided, along with several voice circuits for overall monitor, control, and coordination of the array.

The remaining dedicated equipment is subdivided as follows and is the subject of this report.

(1) The Receiver Subsystem is a single channel telemetry demodulator, accepting an approximate 315-MHz signal at the ESA interface and providing baseband outputs for recording and intersite link transport to CDSCC.

(2) The Recording Subsystem consists of duplicate sets of equipment (at Parkes and at CDSCC) which accept a single channel of baseband telemetry and format it for recording on one or both of two transports. Each transport is fitted with a deformatting channel, such that the Parkes tape and the CDSCC tape can be played back simultaneously for near-real-time processing. The Parkes equipment further provides for radio science input and downconversion, prior to processing through the baseband channel.

(3) The Combining Subsystem provides not only the actual combining at CDSCC, but the interconnect, monitor, and control of the entire system. This includes test signal facilities, link calibration devices, array controllers at both sites for configuration control and tape coordination, and a dedicated array operator position at CDSCC. An additional operator is required intermittently at each site for tape changing and back-up modes of operation.

Performance specifications are provided elsewhere.[1] Such detail will be included herein only as pertinent to the equipment descriptions to follow.

A detailed description of the recording equipment is not available at this writing. Hence, the remainder of this article is devoted to the elements of the real-time implementation.

III. The Receiver

A. General Description

The PCTA receiver is a phase tracking receiver that demodulates telemetry data and provides a telemetry baseband signal for data processing. The receiver has been designed to function at a 64-meter site as an array receiver on missions to the outer planets. The receiver operates in the 300-MHz band. It will accept a signal on any DSN X-band channel that has been translated to the 300-MHz band in a downconverter using a fixed frequency local oscillator signal of 8100 MHz.

A block diagram of the receiver is shown in Fig. 5. The basis for the design is the Block III receiver. In fact, surplus Block III modules are used from the 10-MHz intermediate frequency (IF) amplifier through the carrier tracking loop. To interface with the Block III 10-MHz IF amplifer, a dual conversion module has been added (preamplifer/mixer/IF amplifier). This module converts the incoming 300-MHz band signal to a first IF of 70 MHz and then to the second IF of 10 MHz. Since the carrier tracking loop is composed of Block III modules, the loop characteristics of the receiver are identical to those of the Block III receiver. Further detail may be found in Ref. 1.

B. Unique Features

During routine operations, the receiver is under the control of the receiver microprocessor controller. Instructions to estab-

[1]PCTA System Requirements and Design, JPL internal document 1200-2, Jet Propulsion Laboratory, Pasadena, Calif., April 15, 1984.

lish the receiver configuration, initialization, and tracking routines are generated in the array controller (Combining Subsystem) and transmitted to the receiver controller for execution. The receiver also has the capability of being controlled from a local terminal, using the same I/O port that is normally used for communicating with the Combining Subsystem controller. The receiver is also capable of being switched to a fully manual mode of operation.

The controller provides both control and monitor capability. Control functions include configuration, acquisition of the carrier signal, and tracking of signal dynamics. Some major performance parameters, such as receiver status and signal level, are monitored. Frequency programming allows the local oscillator to provide phase-continuous tracking over a full pass.

A narrowband receiver output provides capabilities of measuring carrier signal-to-noise ratios using both fast Fourier transform (FFT) and Y-factor techniques in real time. Further descriptions follow in Section III.C.

C. Functional Description

1. Telemetry channel. Telemetry detection is performed at the first IF of 70 MHz. Since the second mixer reference frequency obtained from the Block III design is 60 MHz, the first IF could have been either 50 MHz or 70 MHz to obtain a second IF of 10 MHz. Seventy MHz was selected to provide the capability of wider telemetry-channel bandwidth.

At outer planet distances, the telemetry channel is dominated by noise. This is true over the dynamic range of the input signal level. Consequently, it is not necessary to have carrier signal automatic-gain control. However, to operate the telemetry detector most efficiently, at the maximum allowable detector input signal level, it is necessary to provide total power gain control of the telemetry channel in the predetection 70-MHz IF amplifier. This will compensate for any gain changes in the low-noise amplifier and downconverter and for any noise temperature variations due to antenna orientation.

To minimize the effect of phase offsets in the telemetry detector reference signal, which are created in the receiver loop and caused by tracking signal dynamics resulting from Doppler, a phase-error correcting loop operates around the detector. At outer planet distances with planetary fly-by Doppler dynamics, the phase correcting loop reduces the telemetry detector phase error sufficiently to cause no telemetry baseband data degradation.

2. Narrowband channel. A narrowband channel is included in the receiver to provide the capability of making signal-to-noise measurements and to aid in acquisition. To support these two functions, two separate output bandwidths are used: 125 Hz for signal-to-noise measurements and 1250 Hz for acquisition aid. In each case the carrier appears at midband when the receiver is in-lock. One synthesizer is used for the final local oscillator signal for both bandwidths. Consequently, these two outputs cannot be used simultaneously.

When using the 125-Hz output, the final mixer, local oscillator signal is set to 10.0000625 MHz. When the receiver is in-lock, the carrier signal is at 62.5 Hz. This output is used to calculate carrier-to-noise, spectral-density power ratios using Y-factor techniques, both in the computer mode and the manual mode.

When using the 1250-Hz output, the final mixer, local oscillator signal is set at 10.000625 MHz. When the receiver is in-lock, the carrier signal is at 625 Hz. During acquisition in the computer mode, the frequency offset of the carrier from 625 Hz is automatically measured using FFT techniques. A correction is then made to the receiver local oscillator to reduce this frequency offset to less than 10 Hz. The receiver will then automatically acquire the carrier signal. In the manual mode, the same technique is used, using an auxiliary spectrum analyzer. In addition, the frequency offset can be observed by monitoring the dynamic phase error as the signal-to-noise ratio (SNR) in the predetection bandwidth is near unity. The receiver local oscillator can then be adjusted manually until the observed frequency offset is less than 10 Hz, at which time the receiver will automatically acquire the carrier signal.

3. Controller. A simplified block diagram of the Receiver Controller is shown in Fig. 6. The Receiver Controller design is implemented using an Intel SBC 86/14A single-board computer (5-MHz 8086/8087 based), an SBX 488 General Purpose Interface Bus (GPIB) interface controller, an SBX 311 A/D (12 bit) analog-to-digital converter, and an SBC 464 PROM board. The Controller is configured around a standard multibus (IEEE-796) chassis using ±5V and ±12V power.

Upon power-up and after a self-test, the Controller software enters the main loop of the program, which monitors input and processes timer queued tasks. The tasks that are queued by an onboard timer are update and correct system status (once every 3 sec), update sweep frequency, and update autotrack frequency (each once every second). The monitoring of user input is always active.

The main features of the Receiver Controller are the automation of carrier acquisition and signal-to-noise calculations. The Receiver Controller performs a 256-point, real-to-imaginary

FFT calculation on the carrier during the automatic acquisition and during SNR calculations. For additional SNR accuracy, the Y-factor measurement technique is used. The carrier signal level is then calculated from the measured SNR, assuming a 20-Kelvin (or operator updated value) system-noise temperature.

During carrier acquisition, the Controller calculates the expected X-band frequency from the text predict values. These values are entered by the operator during the tracking procedure or prior to tracking. Using these predict values, the Controller calculates and sets the synthesizer frequency based on algorithms similar to those used in the manual mode. The receiver loop is then disabled and 256 samples of the wideband output of the receiver are taken. The predict values will set synthesizer frequency within ±625 Hz of the desired in-lock value, so that the carrier appears in the receiver 1250-Hz output. With 256 samples of the receiver wideband output, the result is an FFT calculation with a 10-Hz bandwidth resolution. An amplitude spectrum is then generated and the assumption is made that the strongest signal in the spectrum is the carrier. The carrier-frequency offset from 625 Hz is calculated, the synthesizer frequency is then corrected for the offset, and the receiver loop enabled. The receiver then acquires the carrier signal and the controller polls the receiver up to 10 seconds for an in-lock indication.

During operation, when the receiver is in the Controller mode, the Controller monitors the status of the receiver. If any error occurs, the Controller will inform the operator via an error message to the terminal. In some instances, the Controller will correct the error and then inform the operator of its occurrence. To aid in the operation of the receiver, a "HELP" menu is available to the operator upon request (Fig. 7).

Spectral displays are available for both the 125-Hz and the 1250-Hz receiver outputs using the same FFT algorithm used in the acquisition procedure. In addition, signal-to-noise, spectral-density calculations are also made using the FFT algorithms.

In addition to the FFT algorithm, a more precise signal-to-noise, spectral-density calculation is available at the receiver 125-Hz output using a Y-factor algorithm. The output is sampled (with the carrier in the spectrum) 256 × 10 times at 4 msec intervals. Using the synthesizer to move the carrier out of the receiver narrowband output spectrum, the output (without carrier in the spectrum) is sampled 256 × 30 times at 4 msec intervals. Using the same type of Y-factor algorithm that is used in the manual mode, the carrier signal-to-noise spectral density is then calculated and displayed.

IV. The Combiner

A. General Description

The function of the Long Baseline Combiner (LBC) is to accept baseband signals from Parkes and CDSCC, to align them properly in time, weight the signals appropriately according to their respective SNRs, and then to sum and output the results. The block diagram in Fig. 8 shows how this is accomplished.

The LBC is similar to the Baseband Assembly (BBA) Real-Time Combiner. The latter consists of two 4-channel combiners, which are cascaded to produce an eight-channel combiner. Since the LBC requires only two channels, and must compensate for larger static and dynamic delays, the internal configuration is different. Due to the similarity of the devices, some of the BBA modules are used in the LBC. These include the analog-to-digital converters (ADC), the clock phase shift (CPS) board, the multiplier-adder board (MAB), the correlator board (CB), and the digital-to-analog converter (DAC). The digital delay board (DDB) is similar to the one in the BBA, but is designed to provide four times the static and dynamic delay capability for a given clock rate.

Requirements for the LBC consist of being able to compensate for 2.4 msec of round-trip transport delay between Parkes and CDSCC (2.4 for testing, only 1.2 for operating), a dynamic delay in excess of ±200 μsec, and a delay rate of 40 nsec/sec. Meeting these requirements, and still maintaining a SNR loss of less than 0.1 dB, required a higher loop-update rate than that used in the BBA. The higher rate was achieved by using a higher speed Intel 86/14 single-board computer utilizing the 8086 microprocessor, with 8087 coprocessor, rather than the Intel 80/204 single-board computer utilizing the 8080 microprocessor, which is used in the BBA.

The signals from Parkes and CDSCC are first low-pass filtered at 4 MHz before being applied to the ADC. This choice of bandwidth is bounded by the need to pass the harmonics of the 360-kHz subcarrier signal and by noise-squaring effects in the correlator (see Section IV.B. below).[2] The 8-bit digitized signals are passed through the DDBs and then to the MAB. The MAB multiplies each signal by a weighting factor based on its SNR, and then adds the signals. The summed signal is then converted back to analog form by the DAC. All modules are under control of the 8086 microprocessor.

[2]This limitation is also related to dynamic range characteristics of the ADC. Had the noise-squaring and attendant signal-suppression effects been more severe, additional (digital) filtering might have been employed in the correlator path.

The feedback loop, which maintains the time alignment of the signals, consists of the DDBs, the CB, a loop filter equation implemented by the microprocessor, the CPS board, and the ADC. Loop design is described in the next section.

B. Combiner Loop Design

1. A delay tracking loop. Having established the memory capacity to satisfy the static delay requirements for the Parkes–CDSCC application (Section IV.A.), the next step was to model the BBA combiner loop hardware. Figure 9a is a hybrid s/z-transform block diagram, developed with the aid of Ref. 2 and personal communication with the author. A significant change from the Mariner–Venus–Mercury (MVM) design [Ref. 2] is that the dynamic delay device and clock provide a delay hold in the interval between loop updates, rather than a frequency (or phase ramp) hold as with a voltage-controlled oscillator. As a direct consequence, the alignment error, τ_e, is a replica of the change in input over the interval T. The sinusoidal geometric delay, $\tau_{IN}(t)$, has a maximum rate of change for the Parkes–CDSCC baseline of 40 nsec/sec. As will be noted later, alignment errors of approximately 10 nsec were budgeted for the 360-kHz square-wave subcarrier application. These factors dictated that the loop update interval and/or the aiding interval, T_{aid}, must be less than one second, the value used for telemetry combiners to date. As will be discussed in Section IV.C., the delay aiding is provided to minimize the tracking requirements upon the loop. A convenient value was found to be $T_{aid} = 0.025$ sec resulting in a negligible, one nanosecond peak-to-peak sawtooth of ramp error, superimposed upon the loop. Thus, the aiding will not be explicitly treated below, except as it mitigates the dynamics of the input.

Another factor, computation time, was considered negligible for engineering purposes, estimated at 10-to-20 msec, given a loop update interval of $T = 0.20$ sec (see Section IV.B.2.) and the insensitivity of performance characteristics established in Ref. 3.

Referring now to Fig. 9b, the open-loop transfer function may be written as

$$G_{OL}(z) = K_c F(z) \frac{z-1}{Tz} \left[\frac{z-1}{zs} \frac{1}{s}\right]^*$$

where $z = e^{Ts}$ and $[\ ]^*$ denotes the z-transform of the bracketed expression.

This yields

$$G_{OL}(z) = K_c \frac{F(z)}{z}$$

where K_c is the (dimensionless) correlator gain and all other gains are lumped in $F(z)$. This simple expression illustrates that the loop type (I or II) will be exactly that of the $F(z)$ employed and that the dominant effect of the remainder of the loop is a transport lag of T sec. It is the latter that gives rise to the gain margin limitation as derived in Appendix A.

A strawman loop filter was postulated (Appendix A) with three generalized parameters A, B, and C as

$$F(z) = \frac{A z^2 + C(z-1)z}{(z-1)(z-B)}$$

resulting in

$$G_{OL}(z) = K \frac{z + \frac{C}{A}(z-1)}{(z-1)(z-B)} \tag{1}$$

where $K = AK_c$. The closed-loop portion of Fig. 9b has the transfer function:

$$G_{CL}(z) \triangleq \frac{\tau_{OUT}(z)}{\left[\frac{\tau_{IN}(s)}{s}\right]^*}$$

$$G_{CL}(z) = \frac{K_c F(z) \frac{z-1}{Tz} \left[\frac{z-1}{zs}\right]^*}{1 + G_{OL}(z)}$$

$$G_{CL}(z) = \frac{K}{T} \frac{(z-1)z + \frac{C}{A}(z-1)^2}{(z-1)[(z-1)+1-B] + Kz + \frac{C}{A}K(z-1)} \tag{2}$$

Appendix A derives expressions for gain margin, damping, and loop bandwidth as presented in Fig. 10. Note that $G_{CL}(z)$ is not the transfer function relating τ_{OUT} to τ_{IN}.

General solutions for steady-state errors are obtained through

$$\tau_e(z) = \tau_{IN}(z) - \tau_{OUT}(z)$$

$$= [\tau_{IN}(s)]^* - \left[\frac{\tau_{IN}(s)}{s}\right]^* G_{CL}(z)$$

and application of the final value theorem. Appendix A derives for all values of filter parameters A, B, and C

$$\left.\begin{aligned} \frac{\tau_\epsilon(ss)}{\Delta\tau} &= 0 && \text{(Delay step)} \\ \frac{\dot{\tau}_\epsilon(ss)}{\dot{\tau}} &= \frac{T}{K}(1-B)-\frac{T}{2} && \text{(Delay ramp)} \\ \frac{\ddot{\tau}_\epsilon(ss)}{\ddot{\tau}} &= \frac{T^2}{K}-\frac{T^2}{K^2}(1-B)-\frac{T^2}{6} && \text{(Delay accel.)} \end{aligned}\right\} \quad (3)$$

Due to the sinusoidal nature of the delay input to the loop, each order of error maximizes when the adjacent order is zero; hence, the expression for delay acceleration does not include the unbounded, integrated ramp error for the type I loop where $B < 1$ (see Appendix A.4). Note that the final term in each case is independent of loop type and gain, K; it represents the value at the update instant and is a consequence of the replica "ripple" discussed above.

2. Choice of loop type. Equation (1) most easily illustrates how the choice of design values for parameters A, B, and C in the filter can yield loops of type I (single integrator) and II (double integrator) with a variety of operational characteristics as illustrated in Eq. (3) and Fig. 10. Over the ranges plotted in this Figure, the straight line asymptotes are valid for engineering purposes. For example, in the (worst-case) region labelled MVM, Eq. (A-4) deviates from the asymptote by 5%.

An initial estimate of the desired loop bandwidth, $2B_L$ = 0.1 Hz, was considered as a compromise between expected jitter losses and transient response at acquisition. Figure 10 and Eq. (3) reveal that the average ramp error for a type I loop (B = 0) at this bandwidth and at T = 1 sec is *five times* the input rate. For example, a two nsec/sec aiding residual (5% of 40 nsec/sec) would yield a 10-nsec steady-state error. This value is on the threshold of acceptable loss for a 360-kHz square wave. While 5% is a rather loose requirement on the ephemeris aiding, a more robust loop was sought to allow for unmodelled errors.

Type II design requires B to be identically one with the C/A ratio establishing the appropriate damping. With the average steady-state ramp error now zero, Fig. 10 points up the need to reduce T in order to obtain adequate gain margin for variations in operating point versus input SNR (adaptive gain and bandwidth) and to allow for unmodelled effects such as computation time discussed above. As noted earlier, a value of T = 0.20 sec was chosen, yielding the upper curve for B = 1 (Fig. 10).

The unaided delay acceleration steady-state error, Eq. (3), is negligible (< 3 nsec) on the Parkes–CDSCC baseline (0.003 nsec/sec^2) for bandwidths greater than about 0.03 Hz, and thus no problem for this design.[3]

Lacking an explicit loss model for loop jitter, several test bandwidths in the range $0.04 \leqslant 2B_L \leqslant 0.50$ were evaluated under design point conditions for degradation of telemetry SNR. Incremental loss for the widest value was within the resolution of the test set-up, 0.1 dB. Hence, a nominal design point bandwidth of $2B_{L_o}$ = 0.25 Hz at a damping of ζ = 1.0 was established as the baseline design for further test and analysis. Figure 11 illustrates this design point and the adaptive range of operability.

The independent variable $SNR_1 SNR_2$ characterizes the correlator input. The input filters were selected as B_N = 4 MHz as a compromise between jitter performance, Appendix A.5, and data spectrum fidelity for the harmonics of 360 kHz. Upstream bandwidths, including that of the microwave link, were specified as 5 to 6 MHz minimum, except the recording equipment which was specified at 3 MHz.

The clear, dry weather SNRs for Voyager/Uranus encounter were nominally +45 and +48 dB-Hz for Parkes and CDSCC respectively, yielding

$$SNR_1 SNR_2 = +45 + 48 - 20 \log 4 \times 10^6 = -39 \text{ dB}^2$$

rounded off to the combiner loop design point value of -40 dB^2 as identified in Fig. 11. The parameter K_{SNR}, also discussed in Appendix A.5, is analogous to the signal suppression factor, α, in continuous loop design, with the significant difference of twice the logarithmic slope due to the squaring effect of two noisy signals in the correlator.

Figure 11 illustrates the adaptive region of operation for design point values of A, B, and C

$$A = 0.0125$$
$$B = 1.00$$
$$C = 0.625$$
$$K_c = 20\,K_{SNR}$$

[3]For the Goldstone and Very Long Array (VLA) baselines, bandwidths are ~0.01 Hz and ~0.1 Hz, respectively.

The upper value of $2B_L$ = 0.45 Hz could conceivably be approached as follows

Nominal SNR_1 SNR_2	–39 (as above)
If Parkes equals DSS-43	+1
Recording bandwidth Δ	+2.5 (1.25 dB each)
Voyager signal uncertainty	+1 (0.5 dB each)
	–34.5 dB^2

Similarly, values of $2B_L$ as low as 0.15 Hz could be obtained near the horizon with rain at one or both sites. Values as low as 0.10 Hz (ζ = 0.5) could be approached only upon degradation of the Voyager signal, but these illustrate loop characteristics in the extreme. The gain margin notation on Fig. 11 illustrates why it is necessary to reduce K by a factor of 10 or more during strong signal testing ($K_{SNR} \rightarrow 1$).

Before turning to a summary of performance for the Parkes–CDSCC long baseline combiner loop, consider the intermediate design (between types I and II) as illustrated in Fig. 10 (dashed lines). This approach sets $C = 0$ and $0 < B < 1$ to satisfy stability criteria, yielding the digital equivalent of an analog "imperfect" second-order loop whose gain is so low as to not require lead compensation. Because selection of B is doubly constrained (ramp error and damping), this configuration is more difficult to optimize than the type II loop.

3. Second-order loop performance. Two significant characteristics remain to be considered for the nominal loop design illustrated in Figs. 10 and 11. First, as a by-product of the steady-state error analysis in Appendix A, the transient responses to a delay step and a delay ramp were obtained by computing the power series in z^{-n} for each pulse response function, $\tau_e(z)$, where the coefficients represent the magnitudes of the time response inverted from the z-domain [Ref. 4, p. 60].

The results are presented in Figs. 12 and 13 and indicate that for loop gain changes of ±2:1 ($\Delta SNR_1\, SNR_2$ of ±6 dB) the loop is well behaved and essentially stabilized at 30 sec. Figure 12 points up the importance of initializing the loop with the best available delay estimate. For example, the ζ = 0.7 response would yield stabilization to 10 nsec in something less than 40 sec for an offset of one μsec and 5 sec for a 0.05 μsec offset. The magnified portion of Fig. 13 illustrates the "ripple" effect and the vanishing average error predicted by Eq. (3) for a delay ramp input.

The remaining performance consideration is loop jitter as a function of K_{SNR} and $2B_L$. From Ref. 3 and Appendix A

$$\sigma_T^2 = \frac{2B_L}{256\, B_N\, f_{sc}^2\, K_{SNR}^2}$$

and with B_N = 4 MHz and f_{sc} = 360 kHz

$$\sigma_T = \frac{\sqrt{2B_L}}{11.52\, K_{SNR}} \text{ nsec} \qquad (4)$$

yielding

	–6 dB $SNR_1\, SNR_2$	Design Point	+6 dB $SNR_1\, SNR_2$
$2B_L$, Hz	0.15	0.25	0.45
K_{SNR}	0.0032	0.0064	0.0128
σ_T, nsec	10.5	6.8	4.5

which are consistent with design goals and test results.

The design thus results in steady-state losses limited to the effects of σ_T and input sampling/filtering losses, which should readily meet the design objective of less than 0.2 dB. The transient responses are seen to be tolerable for rather modest accuracies in initialization and ephemeris aiding and to readily meet the 10-sec design goal under expected conditions.

C. Combiner Firmware

The firmware in the LBC controls the high-speed signal processing boards and also does some of the low-speed signal processing (e.g., some of the tracking loop is in the software). This section describes the choice of computer and compiler and some of the features of the control program that relate to the time alignment of the two input baseband signals and the weighting of those signals to produce the combined output.

Because of the relatively long Parkes–CDSCC baseline, the PCTA geometrical delay can change by as much as 40 nsec/sec. Following the BBA Real-Time Combiner design, it was planned to correct for the known (geometric) delay variations via ephemeris-aiding. This would reduce the dynamics of the signals at the input to the tracking loop and minimize the loop's performance requirements. To assure that the ephemeris-aiding was done sufficiently smoothly so that the dynamics would, in fact, be accurately removed, the LBC firmware had to correct for the geometric delay fairly often, about 10 to 100 times/sec. This put some constraints on the microcomputer speed and on the compiler used. For compatibility with other PCTA controllers, it was also desired that the LBC firmware be written in Pascal MT+86 on an 8086 host computer. (This

presented a conflict since it was also desired to maximize use of BBA code, which was written in FORTRAN. This was resolved by simply translating the relevant procedures into Pascal, guided by an analysis of the combiner signal processing done in the BBA).[4]

Early timing tests showed that the calculations and input/output required for the loop and ephemeris-aiding could not be done from MT+86 alone. An 8087 numerical coprocessor was added to speed up floating-point operations and input/output code segments were rewritten in assembly language to get around these problems. After some experimentation, it was determined that ephemeris-update rates of 100/sec were feasible with this compiler-computer combination, if the machine was not being interrupted with other tasks. The actual rate was then reduced to 40/sec, which was satisfactory for smoothly tracking out the known geometrical delay variations. Since the rate of change of the geometrical delay is sensibly constant over 10 sec, the actual update rate was not recomputed every 0.025 sec, but rather once every 10 sec from the known station and spacecraft positions and the time.

Once it was determined that the 8086/8087/MT+86 combination could support the loop and ephemeris speed requirements, the general structure of the program was patterned after the other PCTA controllers. In the case of the LBC, the program has three interrupt-driven tasks: 1 pps for time, 40 pps for ephemeris aiding (and loop timing), and an asynchronous interrupt for communications input from the PCTA controller. Tasks that were not time critical were then scheduled. The general control flow is an infinite loop which waits for commands from the PCTA control computer. Valid commands then cause procedure calls which execute the commands in *background* to the interrupt procedures.

A useful feature of the LBC firmware is that it allows the combiner to time-share the correlator board between loop operations (i.e., delay tracking) and operations useful for verifying proper symbol alignment, correct combining weights, and ADC adjustments. In the usual situation, the correlator is being used to produce an error signal proportional to the time alignment error of the CDSCC and Parkes signals. This signal is then processed by the loop filter (in firmware) to produce a correction which is applied to the delay boards. This error signal allows the LBC to properly align the signals with respect to the subcarrier; it does not guarantee that the data symbols are correctly aligned. For example, at acquisition, the Parkes data stream might be advanced by one subcarrier period with respect to the CDSCC data due, say, to a slightly incorrect station location entry. The LBC would appear to lock correctly, but the symbols would be misaligned by one subcarrier period and the resulting combined signal would be suboptimum.

The LBC firmware allows a check for this condition. The command "CMAP" suspends loop operations, but maintains the relative alignment of the time series with ephemeris-aiding. During about the next 20 sec (actual integration time is under operator control), the correlator board is reprogrammed to map out the cross-correlation function of the two inputs as a function of relative time lag out to about ±7 μsec. The resulting cross-correlation function CMAP is then plotted on the operator's console, the loop tracking is enabled, and the observed cross-correlation is compared with the expected cross-correlation function under various hypotheses regarding the symbol alignment. These hypotheses are "alignment correct," "one input inverted," "signals misaligned by one subcarrier period," "one signal inverted and signals misaligned by one subcarrier period," "signals misaligned by two subcarrier periods," etc. The choice which best describes the observed cross-correlation function is then printed on the operator's console along with a recommendation for the sequence of commands required to bring the inputs into proper alignment. Figure 14 shows the plot of the temporal correlation function produced by CMAP. Prominent features are the triangle-wave auto-correlation of the square-wave subcarrier, and the decrease in the overall level of correlation at large time lags due to symbol misalignment.

Another feature of the LBC is that it allows independent measurement of the SNRs of its two inputs using the correlator board. Once every 20 sec, the LBC firmware temporarily suspends loop operations and tracks on the ephemeris alone. The correlator board is then reprogrammed to look at the correlation function with an offset of 1.5 subcarrier periods. The difference between the correlation readings at 1 and 1.5 subcarrier periods is proportional to the SNR for that input. This measurement has the advantage that it is independent of some sources of systematic error (notably, DC offset of the ADCs). Of course, this is a measurement of the SNR in whatever the input bandwidth of the data is (e.g., for typical PCTA operating conditions these SNR estimates are on the order of 1%). The LBC firmware allows the operator to specify the differences, if any, in the input bandwidths of the two signals. Using these measured input SNRs (smoothed over any time scale greater than 20 sec and corrected for input bandwidth differences), the LBC can then calculate the optimum weighting factor for the two signals independently of any external instrumentation.

The operator has the option of using the LBC-estimated weighting factor or a weighting factor derived from manually input *a priori* SNRs for the actual combining weights. However, in any case, the LBC-estimated weighting factor is

[4] L. D. Howard, unpublished notes on BBA Real-Time Combiner, 1983.

included in various operator displays and can serve as a check that the relative SNRs of the inputs are near nominal. (Additionally, the LBC is continuously measuring the correlated power – the value of the cross-correlation function at the alignment point. If enabled, an alarm is sounded should this value drop by more than 2 dB. This is a test for catastrophies such as a loss of input, a large reduction in one or both of the input signal's SNRs, a failure of one of the LBC signal processing boards, etc.)

To use the correlator board for the two tasks discussed above, the delay tracking loop must be temporarily suspended. Relative alignment of the signals is maintained via ephemeris-only tracking during these suspensions. The symbol alignment test (CMAP) suspends closed-loop tracking for about 20 sec and is typically called once or twice per pass just after initial acquisition. The SNR-estimating routine is scheduled once every 20 sec and suspends the tracking loop for about 3 sec. Additionally, once every 50 sec the tracking loop is suspended for about 2 sec while the DC offsets in the ADC are measured and the appropriate adjustments are made.

Finally, the LBC firmware allows the operator to call up graphs of the recent correlator error signal versus time (i.e., the input to the tracking loop filter) and the recent delay board corrections versus time (i.e., the output of the tracking loop). These plots proved useful in the design and debugging of the loop filter and in choosing appropriate loop parameters. These plots are also useful in observing the transient response of the loop during acquisition and in determining the extent of (short time-scale) stress on the loop during operations. Included with the plots is also the cumulative closed-loop delay. In the ideal situation, this number is less than one-half of a subcarrier period (i.e., the worst-case delay that had to be added to the ephemeris delay to align the subcarriers). In practice, this is larger due to various inaccuractely modeled delays (for example, due to small errors in effective station or spacecraft locations). This number is useful in determining the slowly varying, systematic delay changes that the loop has to track out.

V. Instrumentation and Control

A. General Description

In the PCTA system, the primary signal-processing elements are the telemetry receiver and the LBC. Once the system is operating, these devices essentially do all of the work.

In order to make these devices easier to use, they are surrounded by monitoring, controlling, and testing equipment. This equipment was designed so as to make the PCTA real-time equipment independent as far as pre-pass system testing and operational monitor and control are concerned, thereby not requiring the use of external resources.

(See Ref. 5 for a more detailed overview. Following is a description of each element and the function it performs.)

B. Array Controller

Overall monitor and control of the PCTA equipment is achieved by using a CPM-86 based multibus microcomputer at each site (Fig. 15). Each device, such as the receiver, combiner, test signal generator, etc., is connected and controlled by the monitor and control computer, or the Array Controller (AC) via an RS-232 interface.

Monitor and control functions reside in all assemblies. Each assembly contains software which makes it stand alone as far as operation is concerned. All assemblies are controlled using the same form of command. They all have self-test capability, command parameter checking, status displays of various parameters as appropriate, and "HELP" menus (Fig. 7).

Residing in the AC is the software which gives it its power. The software has been designed to provide as much power as possible, a user friendly interface, and also a few unique features described below.

The AC at each site is connected to the other via a 4800-baud modem. Using this data link, an operator at Parkes or CDSCC can control all the PCTA real-time equipment from one location. This feature is especially useful when an operator at one site desires the status of assemblies at the other site.

Since the AC is actually a CPM-86-based microcomputer, the operator may generate configuration or command files similar to the familiar submit files used in CPM systems. These configuration files are generated using a standard editor prior to the pass, which the software will execute on command. This capability allows pre-canning of error-prone commands, such as spacecraft and station location used by the LBC, receiver tuning predicts, and switch positions (thereby greatly reducing operator type ins and errors). Standard self-test configuration files are used for system pre-pass testing. An example of a configuration file is shown in Fig. 16. The configuration file capability also includes programmable pauses and looping, which allows operator prompting and periodic automatic status logging.

C. Test Signal Generator

The test signal generator (TSG) (Fig. 17), provides four test signals. One of these is an RF signal which is used by the telemetry receiver. Two are baseband signals used by the Recording Subsystem and also by the combiner. The other

signal is a calibration signal used to assist in the measurement of the transport delay between Parkes and CDSCC. The TSG located at Parkes is the same as at CDSCC; however, not all of the signals are used at a given location.

The TSG uses a 316.8-MHz oscillator which provides the carrier test signal for the receiver. The oscillator drives a phase modulator which, when modulated by a baseband signal, produces a carrier (C) X subcarrier (SC) X data (D) signal. The TSG also contains a RF-noise generator. Summers and front panel attenuators are provided so as to be able to adjust the signal to simulate actual predicted signal levels both in total power and SNR.

The two baseband signal generators each generate a SC X D + noise signal. The subcarrier is generated by dividing down the 316.8-MHz oscillator signal. The data signal is generated in a like manner. The noise generators consist of a 27- or 28-stage digital pseudo-random sequence (PN) generator. The PN generator's long sequence length and high clock rate (16 MHz) produce a noise signal sufficiently flat and free of spectral lines. The two baseband signal generators are identical except that the noise generators are of different length, thereby producing independent noise. Data modulation is selectable between alternating ones and zeros, a PN sequence (length 2048, the same as used in the DSN Test Support Assembly), or none. Like the RF generator, the total power level, as well as the SNR of each baseband generator, is adjustable from the front panel.

The clock to each baseband signal generator comes from a clock deletion circuit. When a clock pulse is deleted, the time difference between the SC X D signals from the two generators is changed. Using this deletion scheme, the TSG can simulate fixed as well as dynamic signal delays. Under control of the built-in microprocessor, the TSG can simulate static and dynamic signals from which the algorithms of the long baseline combiner can be verified. One of the SC X D signals (without the noise) is used to modulate the RF modulator described above.

The TSG also generates a 250-Hz pulse signal, synchronized with the station 1 pps which can be used to measure the microwave link polarity, and transport delay.

Subcarrier rates, data rates, static delay, dynamic delay, etc. are all user controllable via an RS-232 interface from the AC.

D. Subcarrier SNR Estimator

Keeping in line with the philosophy of a stand-alone system, a method of determining the presence and level of a signal in the baseband bandwidth is needed. The Subcarrier SNR Estimator (SSE) (Fig. 18) performs two functions: to determine the frequency of the modulated subcarrier, if present; and to measure the subcarrier-to-noise density ratio.

The SSE operates on a modulated subcarrier with a frequency of 360 kHz and symbol rates up to 60 Ksps. Since it is expected that a randomly modulated subcarrier at the noise level cannot be seen on a standard spectrum analyzer due to the spreading of the subcarrier power, the SSE is necessary.

The input signal is first bandpass filtered at 360 ±30 kHz and gain controlled using a microprocessor-controlled digital attenuator and amplifier. The signal is then input to a squaring circuit consisting of a four-quadrant multiplier which removes the data modulation, and doubles the subcarrier frequency to 720 kHz. The doubled subcarrier frequency is then downconverted to 62 Hz using another four-quadrant multiplier and a microprocessor-controlled frequency synthesizer. The downconverted signal is then passed through a 125-Hz low-pass filter, digitized at 250 sps, and the samples are sent to the microprocessor for processing.

The SSE performs two functions on the digital samples. The first is an FFT on the samples. The FFT is displayed on the cathode ray tube (CRT), thereby showing the spectrum about the subcarrier. The display shows the presence of the signal, the approximate SNR, and the subcarrier frequency offset from 360 kHz. This computation will determine the subcarrier frequency to better than 0.5 Hz, and the absolute SNR to about 2 dB if the SSE is set to the exact subcarrier frequency.

If the signal is approximately centered in the display, the second function, a Y-factor SNR measurement, can be made. The familiar Y-factor method computes SNR by knowing that $S/N = (S + N)/N - 1$. The $S + N$ measurement is made by squaring an ensemble of samples, computing their average, and taking the square root of that average. The N measurement is performed in a like manner, with the exception that the frequency synthesizer is changed so that the signal does not appear in the passband of the low-pass filter. For greater accuracy, the user can control how many averages are taken. The accuracy of this measurement is about 0.5 dB with a subcarrier SNR of 48 dB-Hz.

The SSE is primarily used to verify that proper signals are present at the LBC inputs prior to attempting combining, and to verify combining gain independently of the LBC itself.

E. Switching Assembly

Signal routing between various components of the PCTA system is performed by the switching assembly. The switching assembly contains coax relays, a power splitter, and ampli-

fiers required to maintain the proper signal flow, impedance, and signal levels throughout the system. The coax relays may be controlled manually from front panel switches, but are normally automatically controlled by the AC. Engraved on the switching assembly front panel is a PCTA-system block diagram. The manual control switches and light-emitting diodes (LEDs) are positioned to provide a convenient indication of the signal flow.

References

1. Operations and Maintenance, PCTA Receiver, JPL Technical Manual 03110, Jet Propulsion Laboratory, Pasadena, Calif., July 1, 1984.
2. Winkelstein, R. A., "Analysis of the Signal Combiner for Multiple Antenna Arraying," *DSN Progress Report 42-26*, Jet Propulsion Laboratory, Pasadena, Calif., pp. 102–118, April 15, 1975.
3. Simon, M. K., and Mileant, A., "Performance Analysis of the DSN Baseband Assembly (BBA) Real-Time Combiner (RTC)," JPL Publication 84-94, Jet Propulsion Laboratory, Pasadena, Calif., May 1, 1985.
4. Ragazzi, J. R., and Franklin, G. F., *Sampled-Data Control Systems*, McGraw-Hill, New York, 1958.
5. Parkes–CDSCC Telemetry Array, Users' Guide, JPL Technical Manual 513957, Jet Propulsion Laboratory, Pasadena, Calif.

Fig. 1. Parkes Radio Telescope

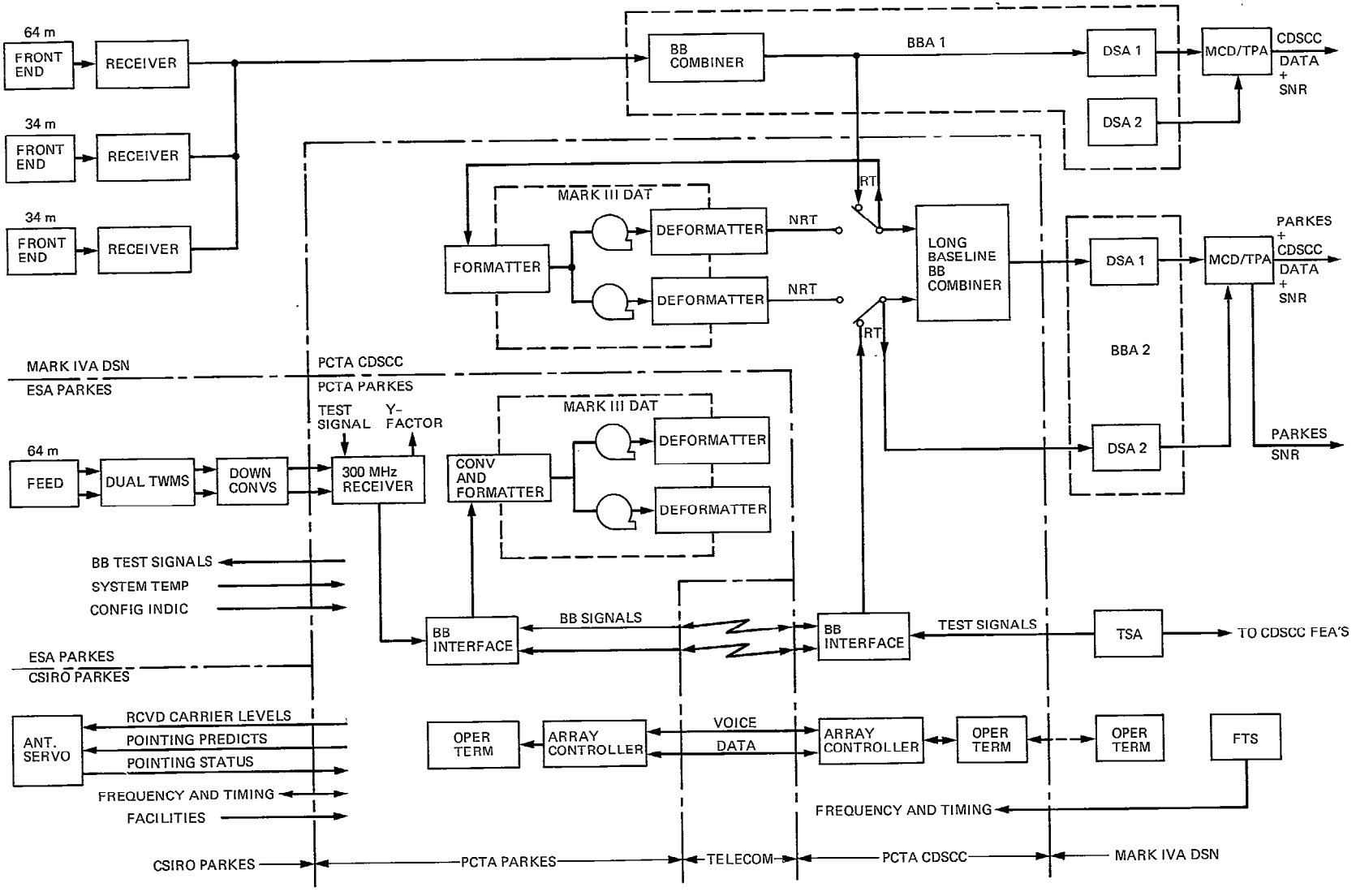

Fig. 2. Parkes-CDSCC Telemetry Array, functional block diagram

Fig. 3. Parkes X-band feedhorn

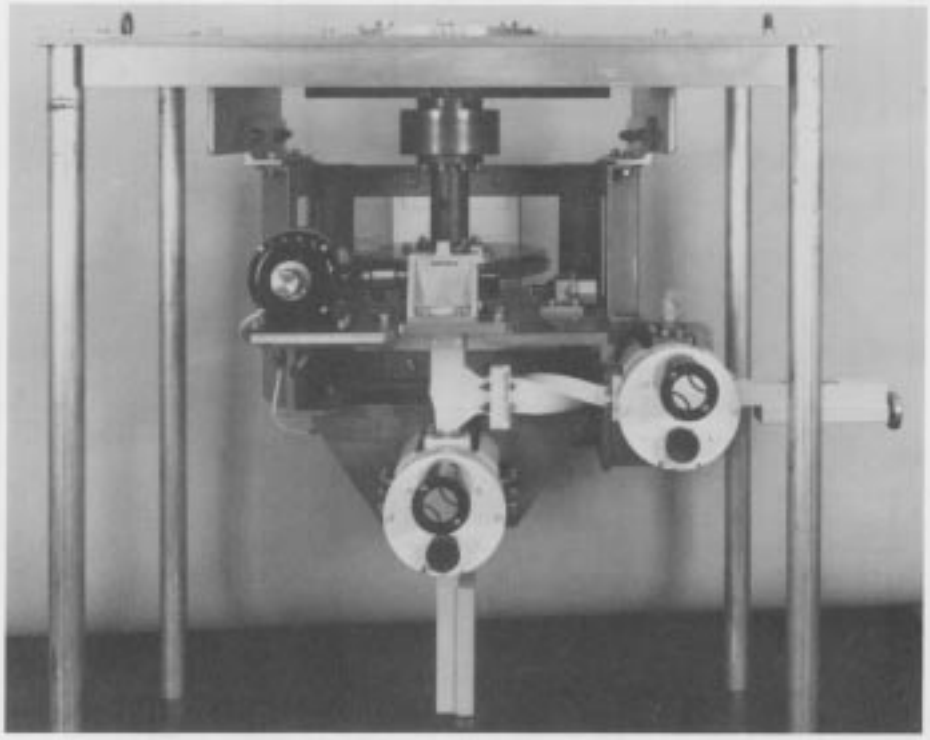

Fig. 4. X-band microwave assembly

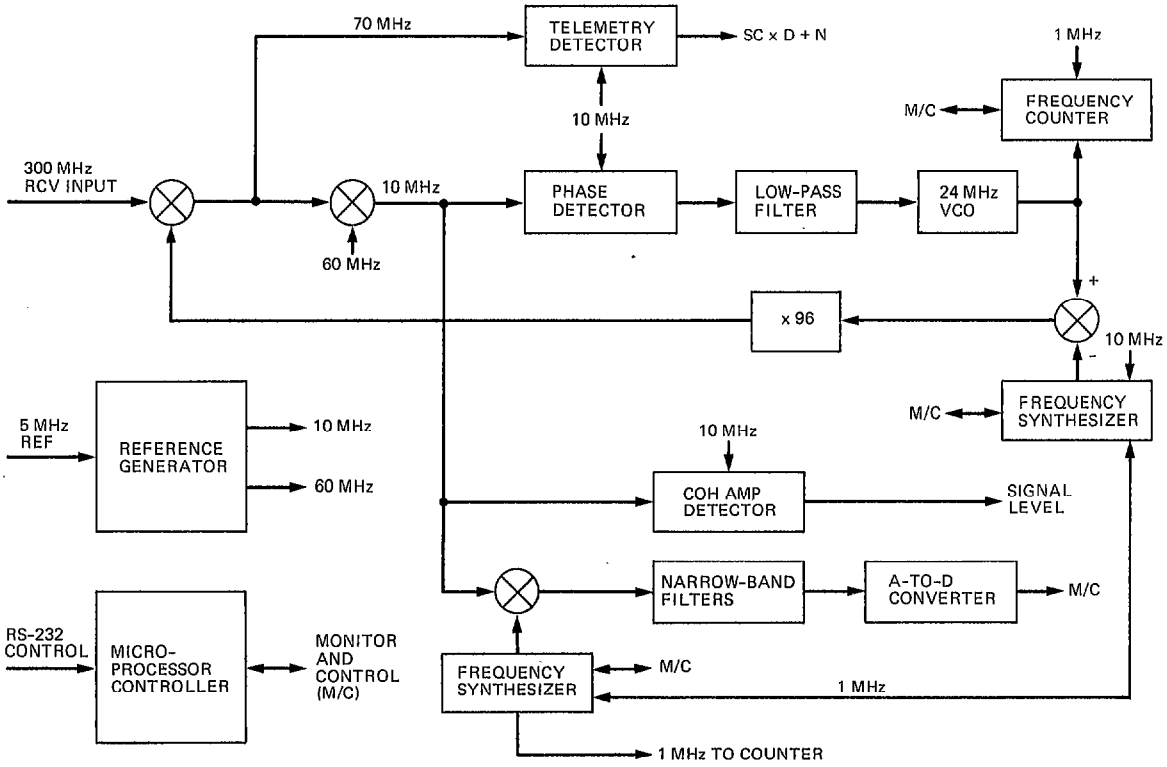

Fig. 5. Receiver block diagram

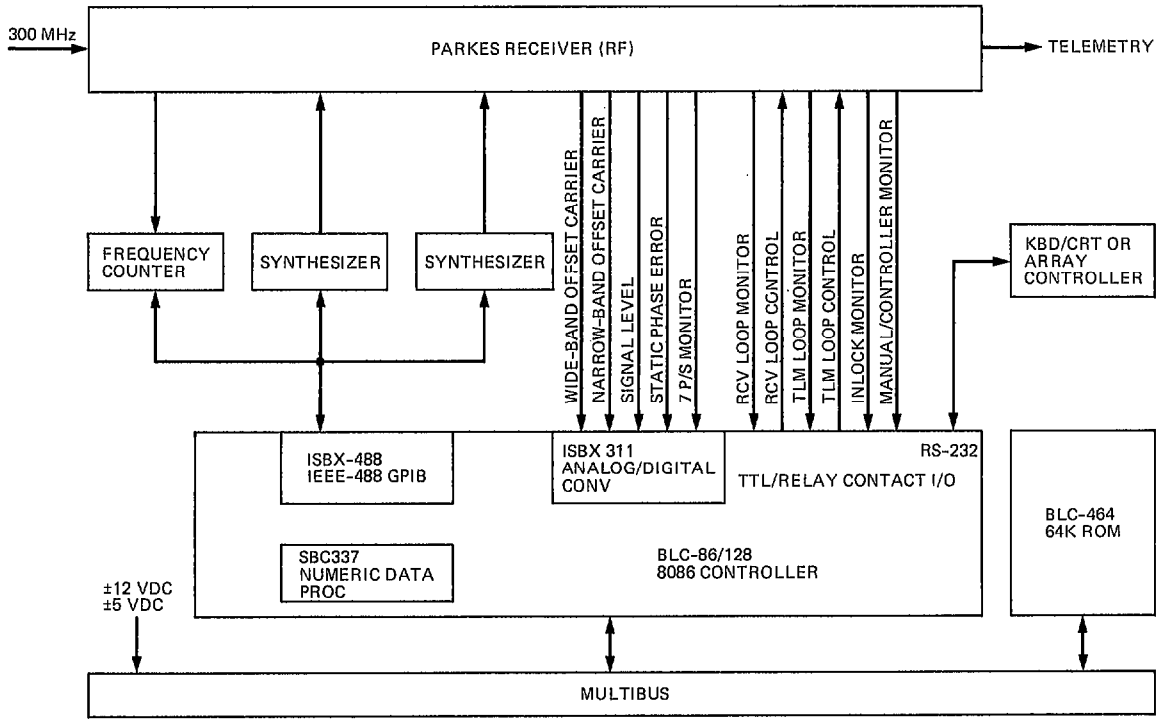

Fig. 6. Receiver controller block diagram

```
PRCV help . . .
The format for user input is: <COMMAND>:<DATA OR OPTION>

THE COMMANDS ARE:

INIT  : <Init Rcvr subsystem. Options NONE or S (self-test) or H (HPIB)>
TSFR  : <Enter predix track freq in HZ, KHZ or MHZ or>
        <TEST option (use test valves for TSF & doppler)>
DOPP  : <Enter predix doppler freq in HZ, KHZ or MHZ. Options NONE>
SFSR  : <Enter sweep rate. Options NONE>
SPEC  : <Display carrier spectrum & SNR. Options are>
        <N (nb), W (wb) or P (wideband using predix)>
STAT  : <Options V (volt), P (phase), M (mode), 0
        <1 (synth 1 freq), C (carrier signal level) & D (predix/VCO)>
ECHO  : <Options ON or OFF>
RLEN  : <Rcvr loop ENABLE or DISABLE>
ACQR  : <Initiate automatic carrier acquisition.>
        <Option P (acquire using last entered predix valves)>
ATRK  : <Initiate auto-tracking. Options ON or OFF>
TLEN  : <Telemetry loop ENABLE or DISABLE>
YSNR  : <Calculate Y-factor SNR and power of carrier. Options NONE>
STMP  : <Enter system temperature (assumed to be in degrees Kelvin)>
MLEV  : <Enter SNR monitor threshold level (assumed to be in dB)>
HELP  : <Display help menu. Options NONE>
```

Fig. 7. Help menu, Parkes receiver

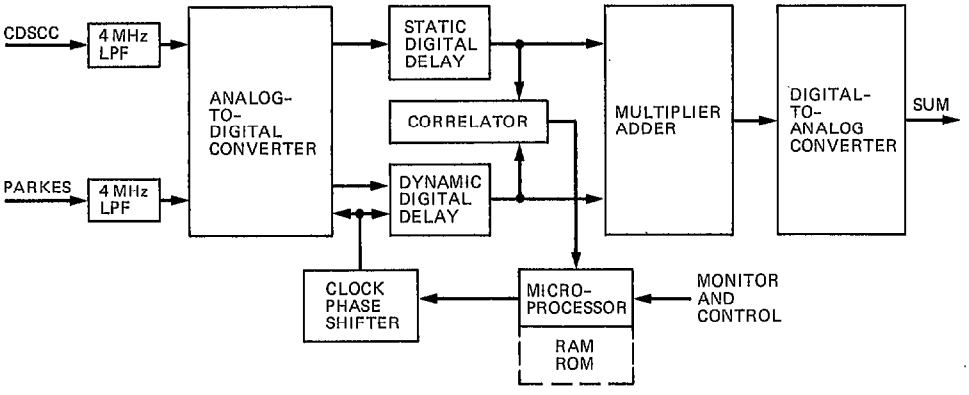

Fig. 8. Combiner block diagram

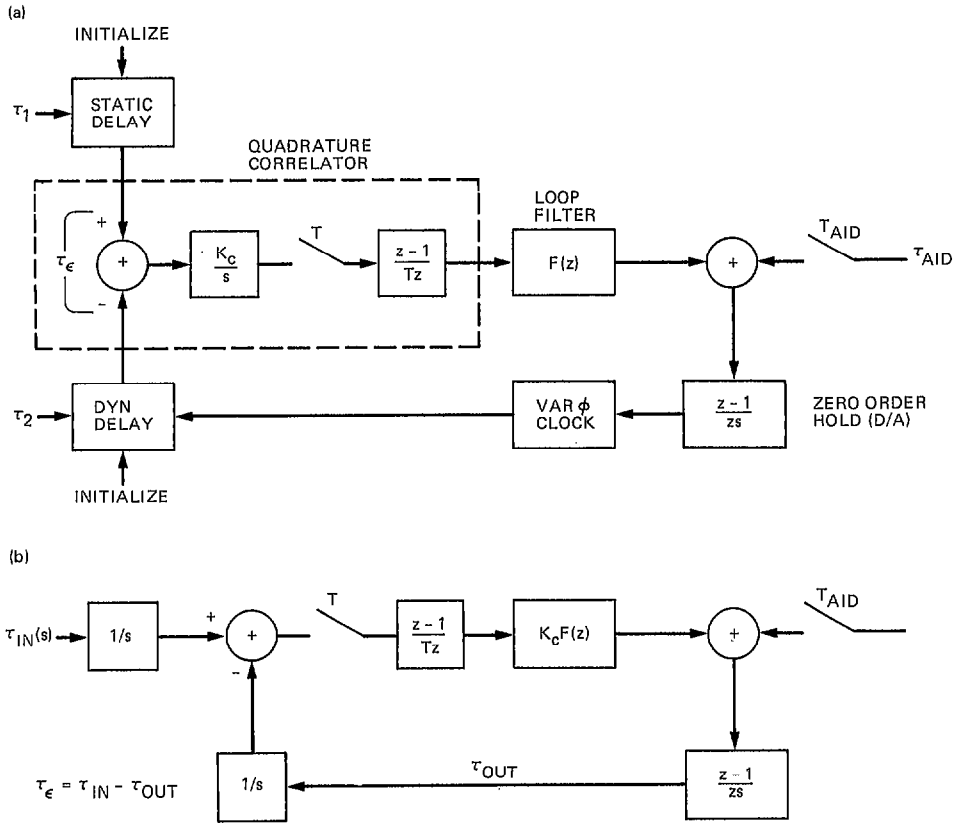

Fig. 9. Loop diagrams (a) hybrid and (b) equivalent error sampled

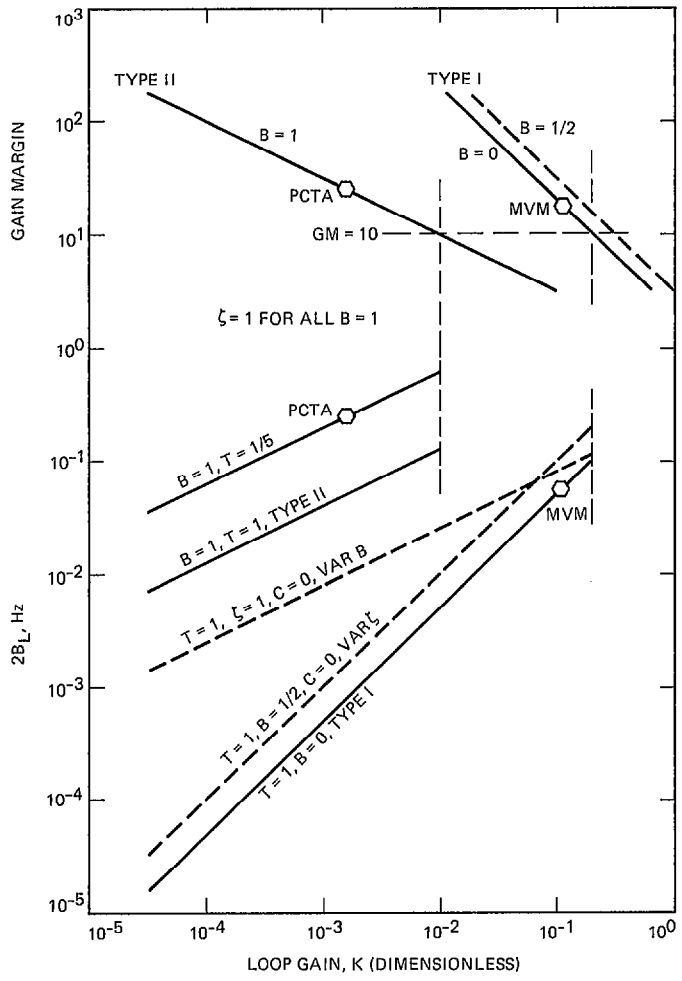

Fig. 10. Loop bandwidth and gain margin

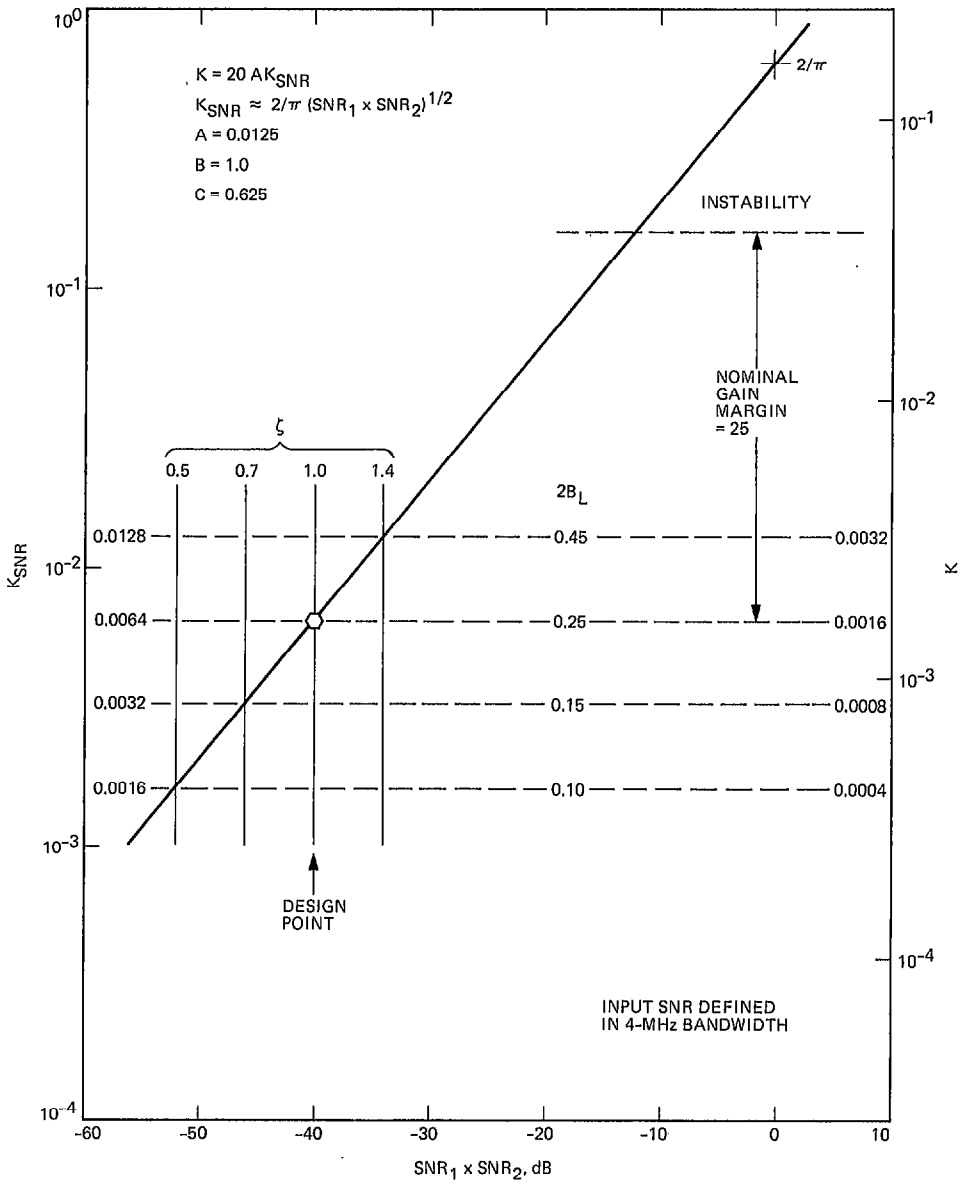

Fig. 11. Loop gain versus input SNR

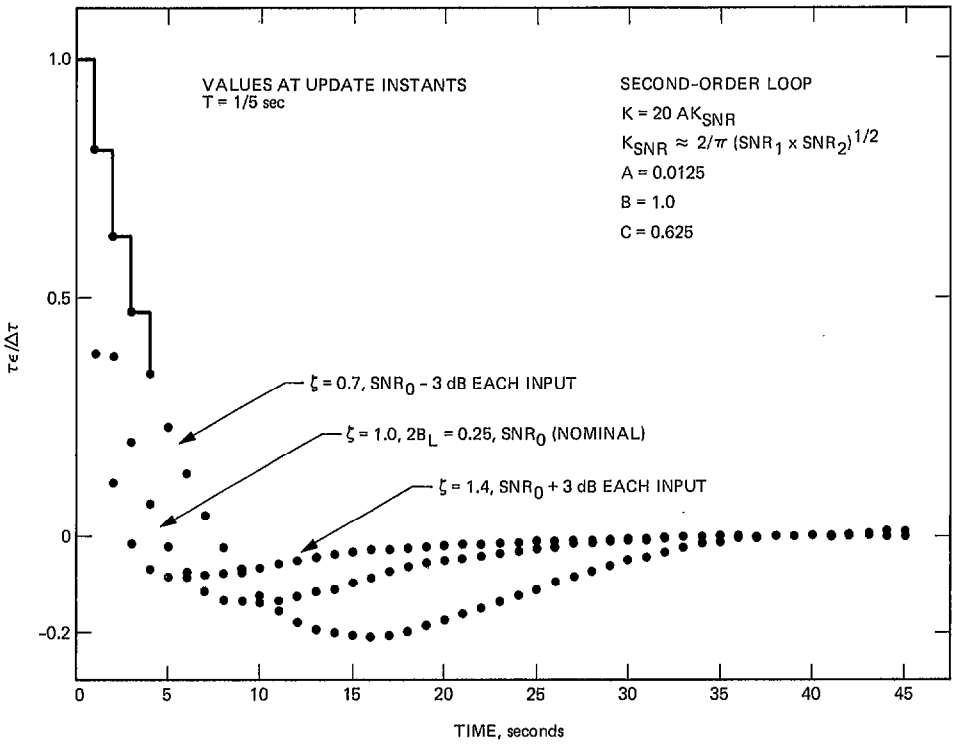

Fig. 12. Transient step response versus input SNR

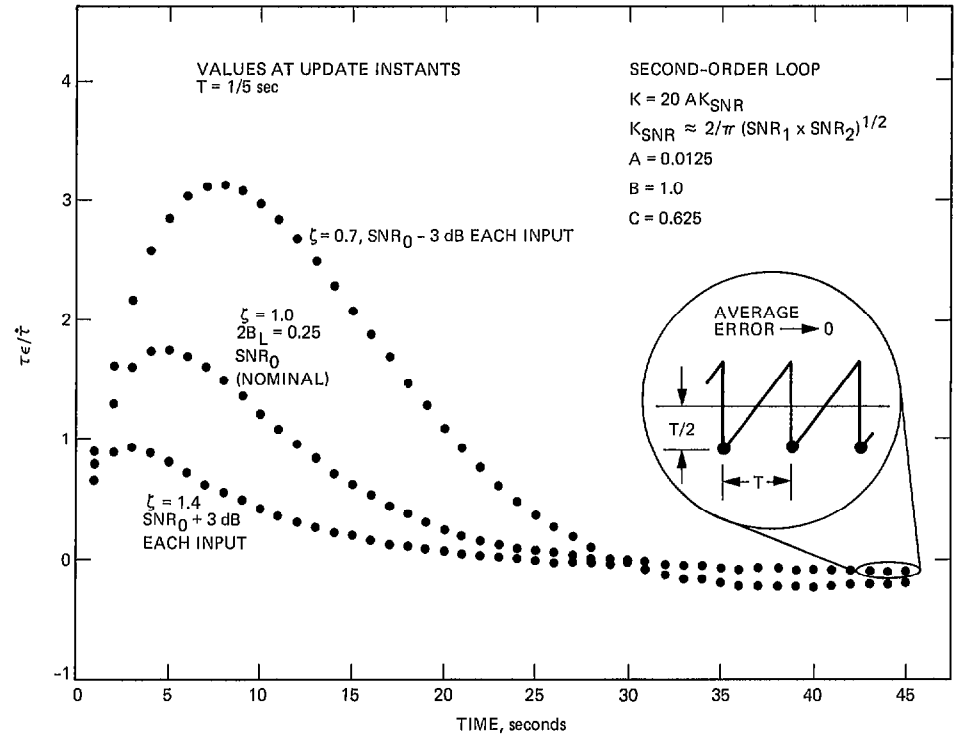

Fig. 13. Transient ramp response versus input SNR

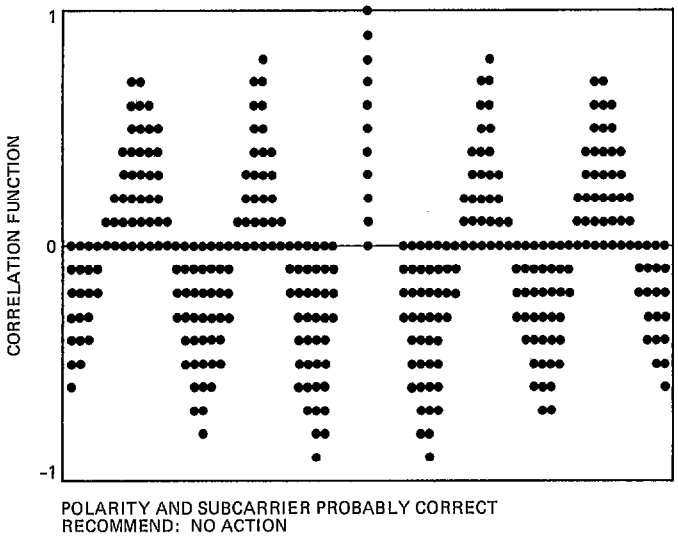

Fig. 14. CMAP display

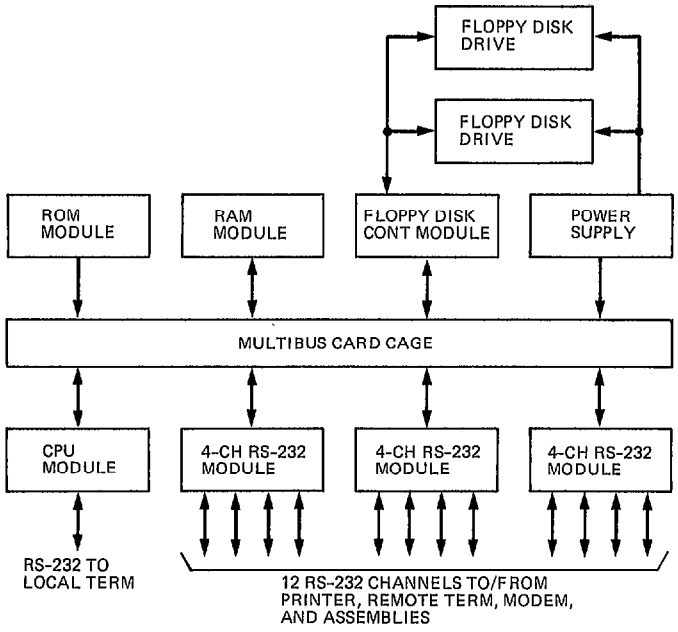

Fig. 15. Array controller block diagram

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- - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
                    OPERATIONAL MODE
LIVE SIGNAL COMBINING AND RECORDING - OPRMOD.CNF

                    LAST UPDATE 01/16/85
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

OPERATIONAL MODE COMMAND CONFIGURATION FILE (LIVE SIGNAL COMBINING AND REC-
ORDING) FOR SWITCHING ASSEMBLY SIGNAL ROUTING, TEST SIGNAL GENERATOR CONTROL
COMMANDS, PCTA COMBINER CONTROL COMMANDS AND RECEIVER CONTROL COMMANDS.


********** CDSCC SIGNAL ROUTING CONFIGURATION - [ CSAM ] COMMANDS **************

CDSCC COMBINER INPUT SELECT <1 I 2 I 3 I 4 I 5>
CSAM:S1:4

LINK INPUT SELECT <1 I 2 I 3>
CSAM:S2:3

PARKES COMBINER INPUT SELECT <1 I 2 I 3>
CSAM:S3:2

PARKES SIGNAL POLARITY SELECT <1 I 2>
CSAM:S4:2

LINK OUTPUT SELECT <1 I 2 I 3 I 4 I 5 I 6>
CSAM:S8:6

********** PARKES SIGNAL ROUTING CONFIGURATION - [ PSAM ] COMMANDS *************

LINK OUTPUT SELECT <1 I 2 I 3 I 4>
PSAM:S1:4

RECORDER INPUT SELECT <1 I 2>
PSAM:S2:2

RECEIVER INPUT SELECT <1 I 2 I 3>
PSAM:S3:3

********** CDSCC TEST SIGNAL GENERATOR CONFIGURATION - [ CTSG ] COMMANDS*******

SET HIGH FREQUENCY NOISE <ON I OFF>
CTSG:RFNS:OFF

SET HIGH FREQUENCY CARRIER <ON I OFF>
CTSG:RFCR:OFF

********** PARKES RECEIVER - [ PRCV ] COMMANDS ***********************************

SET BLOCK IN RECEIVE FREQUENCY PREDICT <41.8 - 44.0 MHz I TEST>
PRCV:REFR:TEST

SET AUTO TRACK MODE <ON I OFF>
PRCV:ATRK:OFF

SET LINEAR SWEEP <0 TO 9 Hz>
PRCV:SFBR:0

SET ISS LOOP SHORT <ENABLE I DISABLE>
PRCV:RLEN:DISABLE

****** CANBERRA LONG BASELINE COMBINER CONFIGURATION - [ CLBC ] COMMANDS ****

SET LINK DELAY <MICROSECONDS>
CLBC:LDLY:0.0

SET BBA THROUGHPUT DELAY <MICROSECONDS>
CLBC:SDLY:0.0

SET CLOCK OFFSETS <+ OR - NUMBER MICROSECONDS>
CLBC:SDLY:0.0

SET YEAR OF OBSERVATIONS <YYYY>
CLBC:YEAR:1982
```

Fig. 16. Sample configuration file

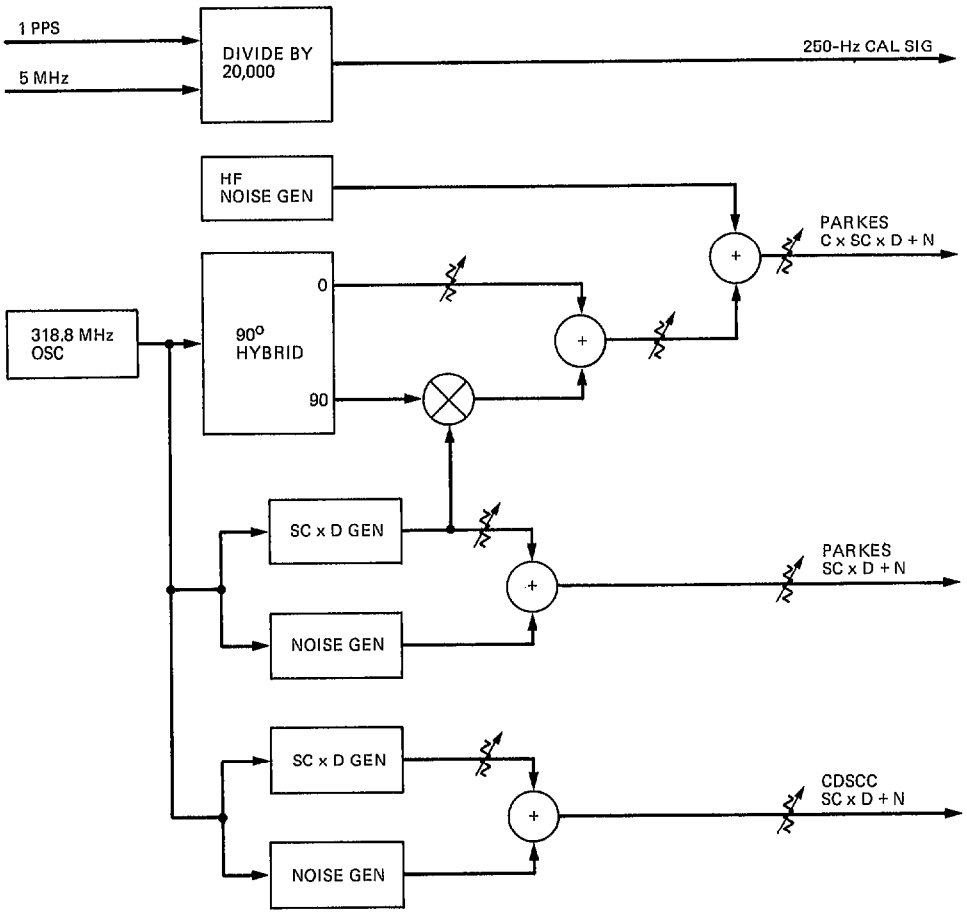

Fig. 17. Test signal generator block diagram

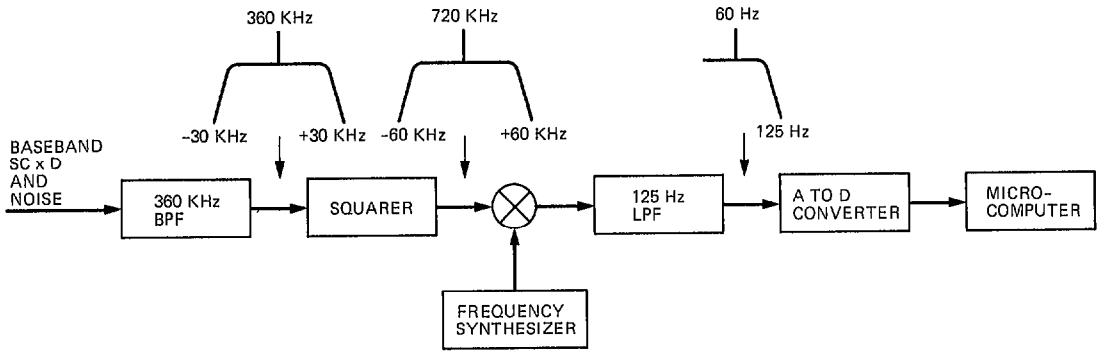

Fig. 18. Subcarrier SNR estimator block diagram

Appendix A
Combiner Loop Analysis

I. Generalized Loop Filter

Consider a sampled-data loop filter. If the output delay τ_i at the ith instant is formed by updating the previous value

$$\tau_i = \tau_{i-1} + \Delta\tau_i$$

and if the update is formed from the input τ_x as follows

$$\Delta\tau_i = A\,\tau_{x_i} + B\,\Delta\tau_{i-1} + C(\tau_{x_i} - \tau_{x_{i-1}})$$

the filter output is

$$\tau_i = \tau_{i-1} + A\,\tau_{x_i} + B(\tau_{i-1} - \tau_{i-2}) + C(\tau_{x_i} - \tau_{x_{i-1}})$$

Converting this difference equation to z-transform notation

$$\tau = \tau z^{-1} + A\,\tau_x + B\,\tau(z^{-1} - z^{-2}) + C\,\tau_x(1 - z^{-1})$$

yields

$$F(z) = \frac{\tau}{\tau_x} = \frac{Az^2 + C(z-1)z}{(z-1)(z-B)} \qquad \text{(A-1)}$$

Note that the parameter C of Ref. 3 is unrelated to the parameter C herein.

II. Stability Criteria and Gain Margin

Setting to zero the denominator of Eq. (2) yields the characteristic equation

$$D(z) = z^2 - \left[1 + B - K\left(1 + \frac{C}{A}\right)\right]z + B - \frac{C}{A}K = 0$$

for which stability criteria are

$$D(1) > 0\text{: } K\left(1 + \frac{C}{A}\right) > K\frac{C}{A}$$

or $K > 0$ (negative feedback)

$$D(-1) > 0\text{: } 1 + B > \frac{K}{2}\left(1 + 2\frac{C}{A}\right)$$

$$\text{Gain Margin} \triangleq \frac{2(1+B)}{K\left(1 + 2\frac{C}{A}\right)} \qquad \text{(A-2)}$$

$$D(0) < 1\text{: } K\frac{C}{A} > B - 1$$

or, by Eq. (A-3), $\zeta > 0$ (damping).

III. Continuous Equivalent Loop Parameters

Given the closed loop transfer function, Eq. (2)

$$G_{CL}(z) = \frac{K}{T}\,\frac{(z-1)\,z + \frac{C}{A}(z-1)^2}{(z-1)[(z-1) + 1 - B] + Kz + \frac{C}{A}K(z-1)}$$

and letting

$$1 - z^{-1} = 1 - e^{-Ts} \to Ts \quad \text{and } z \to 1$$

the continuous equivalent loop is defined for the update rate $(1/T)$, which is large compared with the frequencies of interest

$$G_{CL}(s) \approx \frac{s\left(1 + \frac{C}{A}Ts\right)}{1 + \frac{T}{K}\left(1 - B + \frac{C}{A}K\right)s + \frac{T^2}{K}s^2}, \quad B > 0$$

and from Fig. 9b

$$H(s) = \frac{\tau_{OUT}(s)}{\tau_{IN}(s)} = \frac{1}{s}G_{CL}(s)$$

$$H(s) \approx \frac{1 + \frac{C}{A}Ts}{1 + \frac{T}{K}\left(1 - B + \frac{C}{A}K\right)s + \frac{T^2}{K}s^2}, \quad B > 0$$

By direct analogy with continuous loop analysis, ω_N^2, ζ, and $2B_L$ are defined

$$\left.\begin{aligned} \omega_N^2 &\triangleq \frac{K}{T^2} \\ \zeta &\triangleq \frac{1 - B + \frac{C}{A}K}{2\sqrt{K}} \end{aligned}\right\} \quad B > 0$$

$$2B_L \triangleq \left(\zeta + \frac{1}{4\zeta}\right)\sqrt{\frac{K}{T^2}} = \frac{K}{2T}\left(\frac{C}{A} + \frac{1}{\frac{C}{A}K}\right), \quad B = 1 \qquad \text{(A-3)}$$

For $B = C = 0$ (Type I)[5]

$$2B_L = \frac{K}{2T}\left(\frac{1}{1 - \frac{K}{2}}\right) \qquad \text{(A-4)}$$

Finally, for $0 < B < 1, C = 0$ [Ref. 3]

$$2B_L = \frac{K}{2T}\left(\frac{1}{1 - B}\right) \text{ for } \frac{T_{comp}}{T} << 1 \text{ and } K << 1 \qquad \text{(A-5)}$$

IV. Steady-State and Transient Errors

Owing to the configuration of Fig. 9b, overall $H(z)$ cannot be specified without defining the input $\tau_{IN}(s)$. Accordingly, the loop error is written as

$$\tau_\epsilon(z) = \tau_{IN}(z) - \tau_{OUT}(z)$$

$$= [\tau_{IN}(s)]^* - \left[\frac{\tau_{IN}(s)}{s}\right]^* G_{CL}(z)$$

A. Step Response

For $\tau_{IN}(t) = \Delta\tau$

$$\frac{\tau_\epsilon(z)}{\Delta\tau} = \left[\frac{1}{s}\right]^* - \left[\frac{1}{s^2}\right]^* G_{CL}(z)$$

$$\frac{\tau_\epsilon(z)}{\Delta\tau} = \frac{(z - B)z}{(z - 1)(z - B) + Kz + \frac{C}{A}K(z - 1)} \qquad \text{(A-6)}$$

[5]Winkelstein, R. A., "Long Baseline Combiner Type I Loop Analysis," JPL internal document, *IOM 331-84-272A*, July 31, 1984.

The steady-state error

$$\frac{\tau_\epsilon(ss)}{\Delta\tau} = \lim_{z \to 1}\left\{\frac{z - 1}{z}\frac{\tau_\epsilon(z)}{\Delta\tau}\right\} = 0$$

for all filter forms, due to the $z/(z - 1)$ integration factor in Eq. (A-1) above.

B. Ramp Response

For $\tau_{IN}(t) = \dot{\tau}t$

$$\frac{\tau_\epsilon(z)}{\dot{\tau}} = \left[\frac{1}{s^2}\right]^* - \left[\frac{1}{s^3}\right]^* G_{CL}(z)$$

$$\frac{\tau_\epsilon(z)}{\dot{\tau}} = \frac{Tz}{(z - 1)^2} - \frac{KT}{2}\frac{(z + 1)z^2 + \frac{C}{A}(z + 1)(z - 1)z}{(z - 1)^3(z - B) + K(z - 1)^2 z + \frac{C}{A}K(z - 1)^3} \qquad \text{(A-7)}$$

The steady-state error

$$\frac{\tau_\epsilon(ss)}{\dot{\tau}} = \lim_{z \to 1}\left\{\frac{z - 1}{z}\frac{\tau_\epsilon(z)}{\dot{\tau}}\right\}$$

$$\frac{\tau_\epsilon(ss)}{\dot{\tau}} = \frac{T}{K}(1 - B) - \frac{T}{2} \qquad \text{(A-8)}$$

C. Acceleration Response

For $\tau_{IN}(t) = \frac{1}{2}\ddot{\tau}t^2$ and proceeding as above

$$\frac{\tau_\epsilon(z)}{\ddot{\tau}} = \left[\frac{1}{s^3}\right]^* - \left[\frac{1}{s^4}\right]^* G_{CL}(z)$$

except setting $C = 0$ for simplicity

$$\frac{\tau_\epsilon(z)}{\ddot{\tau}} = \frac{T^2}{6}\frac{3(z + 1)z[(z - 1)(z - B) + Kz] - K(z^2 + 4z + 1)z^2}{(z - 1)^4(z - B) + K(z - 1)^3 z} \qquad \text{(A-9)}$$

This restriction will not affect the steady-state result below (by the continuous analogy).

To obtain the steady-state acceleration error, the limit ($z \to 1$) of Eq. (A-9) above will not suffice, since it is unbounded due to the integrated ramp error of the $B < 1$ loop configurations. Employing the artifice of subtracting out this ramp error prior to taking the limit, the *instantaneous* steady-state acceleration error is obtained for the general case

$$\frac{\tau_e(ss)}{\ddot{\tau}} \triangleq \lim_{z \to 1} \left\{ \frac{z-1}{z} \left[\frac{\tau_e(z)}{\ddot{\tau}} - \frac{\tau_e(ss)}{\dot{\tau}} [t]^* \right] \right\}$$

After substitution, cancellation, and differentiation, Eq. (A-10) is finally obtained

$$\frac{\tau_e(ss)}{\ddot{\tau}} = \frac{T^2}{K} - \frac{T^2}{K^2}(1-B) - \frac{T^2}{6} \qquad \text{(A-10)}$$

The total *growing* steady-state error as a function of time can be synthesized as

$$\frac{\tau_e(ss)}{\ddot{\tau}}(t) = \left[\frac{T^2}{K} - \frac{T^2}{K^2}(1-B) - \frac{T^2}{6} \right] + \left[\frac{T}{K}(1-B) - \frac{T}{2} \right] t$$

which must be interpreted with care. The "real world" separates the components of this error by virtue of the sinusoidal delay variation in which the maxima are separated by six hours.

V. Loop Jitter

From Ref. 3, Eq. (53)

$$\sigma_N^2 = \frac{B_L T_L N_s}{K f_p^2} \left\{ [\text{erf}\sqrt{\text{SNR}_1}\ \text{erf}\sqrt{\text{SNR}_2}]^{-2} - 1 \right\}$$

where N_s is the number of Nyquist samples per symbol and K is the number of symbols per update period T_L, such that

$$\frac{N_s}{K} = \frac{2B_N T_s}{T_L/T_s} = 2B_N T_s^2/T_L$$

where B_N = noise bandwidth of the correlator input.

Also

$$f_p^2 \approx 16 \left(\frac{N_s}{N_{sc}} \right)$$

for low symbol-rate-to-subcarrier ratio and/or low data-transition probability [Ref. 3, Eq. (22)], where N_{sc} = number of Nyquist samples per subcarrier period, such that

$$\frac{N_s}{N_{sc}} = \frac{T_s}{T_{sc}}$$

Substituting all of the above in Eq. (53) of Ref. 3

$$\sigma_N^2 = \frac{B_L B_N}{8 f_{sc}^2} \left(\frac{1}{4K_{SNR}^2} - 1 \right) \approx \frac{B_L B_N}{32 f_{sc}^2 K_{SNR}^2}$$

for low SNRs (defined in correlator input bandwidth) and

$$K_{SNR} \triangleq \frac{1}{2} \text{erf}\sqrt{SNR_1}\ \text{erf}\sqrt{SNR_2} \qquad \text{(A-11)}$$

K_{SNR} may be considered as the noise-dependent factor of K_c, the correlator gain. For all cases of interest, i.e., low SNR

$$K_{SNR}^2 \approx \frac{4}{\pi^2} SNR_1\, SNR_2 \qquad \text{(A-12)}$$

and

$$\sigma_N^2 \approx \frac{\pi^2}{128} \frac{B_L B_N}{f_{sc}^2\, SNR_1\, SNR_2}$$

Converting from Nyquist variance to time

$$\sigma_T^2 = \left(\frac{\sigma_N}{2B_N} \right)^2 \sec^2$$

$$\sigma_T^2 \approx \frac{2B_L}{256\, B_N f_{sc}^2 K_{SNR}^2}$$

$$\approx \frac{\pi^2}{1028} \frac{2B_L}{B_N f_{sc}^2\, SNR_1\, SNR_2} \sec^2 \qquad \text{(A-13)}$$